ABSTRACT

A semiconductor device capable of improving the flexibility of designing electrical lead patterns for connection from chips via a substrate to external terminals by appropriately arranging the substrate structure and layout of more than one address signal as commonly shared by four separate chips is disclosed. In a surface mount type package of ball grid array (BGA), four chips 1 are mounted on a substrate 2 in such a manner such these are laid out in the form of an array of two rows and two columns. These four chips 1 are such that regarding the upper side and lower side, these are in linear symmetry with respect to a center line extending in a direction along long side edges of the substrate 2. Each chip 1 has a plurality of pads 9 which are disposed thereon into an almost linear array substantially along the center line in the direction of short side edges, which pads include addressing pads 9a that are located on the side of central part on a specified plane of the substrate 2, and control-use pads 9b of control signals that are also placed on the center side of the substrate 2. The pad array also includes input/output pads 9c that are disposed so that these are on the peripheral side on the surface of substrate 2.